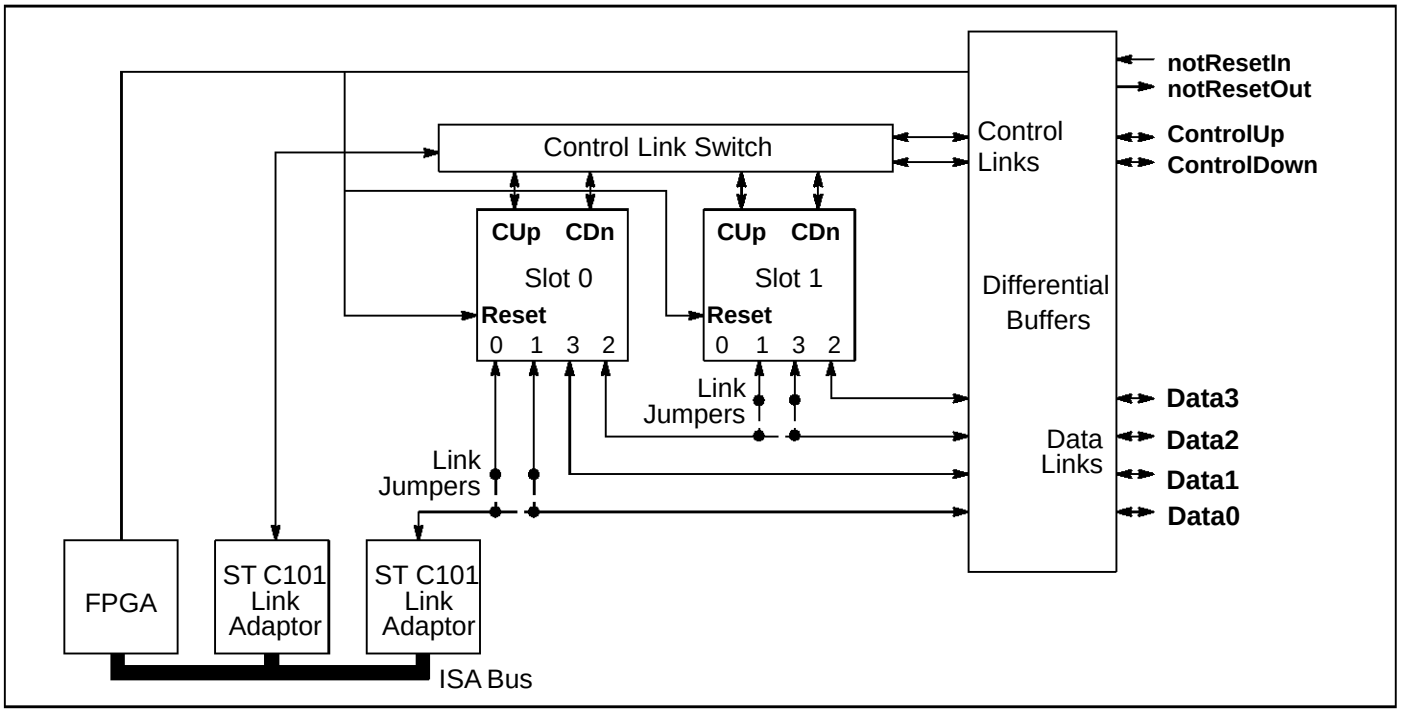
SGS-THOMSON MICROELECTRONICS

IMS B108

PC HTRAM MOTHERBOARD



FEATURES

- High performance DS-Link adaptor based PC bus interface.
- Two logical, size 4, HTRAM slots.
- Standard control and data link interface to T9000 network, either internal or external.
- Control link pipeline jumpering of unused slots.
- Software included supports INMOS PC hosted development tools and user applications.
- Four data DS-Links and two control DS-Links, plus **ResetIn/Out** available on modular connectors.

DESCRIPTION

The IMS B108 is a full length PC-AT format HTRAM motherboard which supports up to two size 2 or size 4 HTRAMs. It also provides a standard control and data DS-Link interface between the PC-AT bus and a T9000 network. The DS-Link interfaces are provided by two ST C101 DS-Link adaptor devices directly interfaced to the PC bus. One ST C101 device is used as the root of a control link network used to configure and control T9000 devices. The second ST C101 device is used as a data link for all application data communication with a PC-based server.

The control link network of the IMS B108 is in the form of a re-configurable pipeline to allow un-used HTRAM slots to be bypassed. Two DS data links are taken from each HTRAM slot through differential buffers to DS-Link modular connectors on the back of the board to allow IMS B108s to be connected to a larger T9000 network. The IMS B108 can therefore support small networks of HTRAMs which are wholly inside the PC host, T9000 networks which are wholly external to the PC, or a network that is both internal and external.

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1.1 IMS B108 hardware specification

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The IMS B108 hardware description consists of the following major sections:

- The control and data DS-Link interfaces, and PC bus interface.
- Data link network and HTRAM slots.
- Control link network.
- External connections

A block diagram of IMS B108 circuitry is shown in figure 1.1 and physical board layout is shown in figure 1.2.

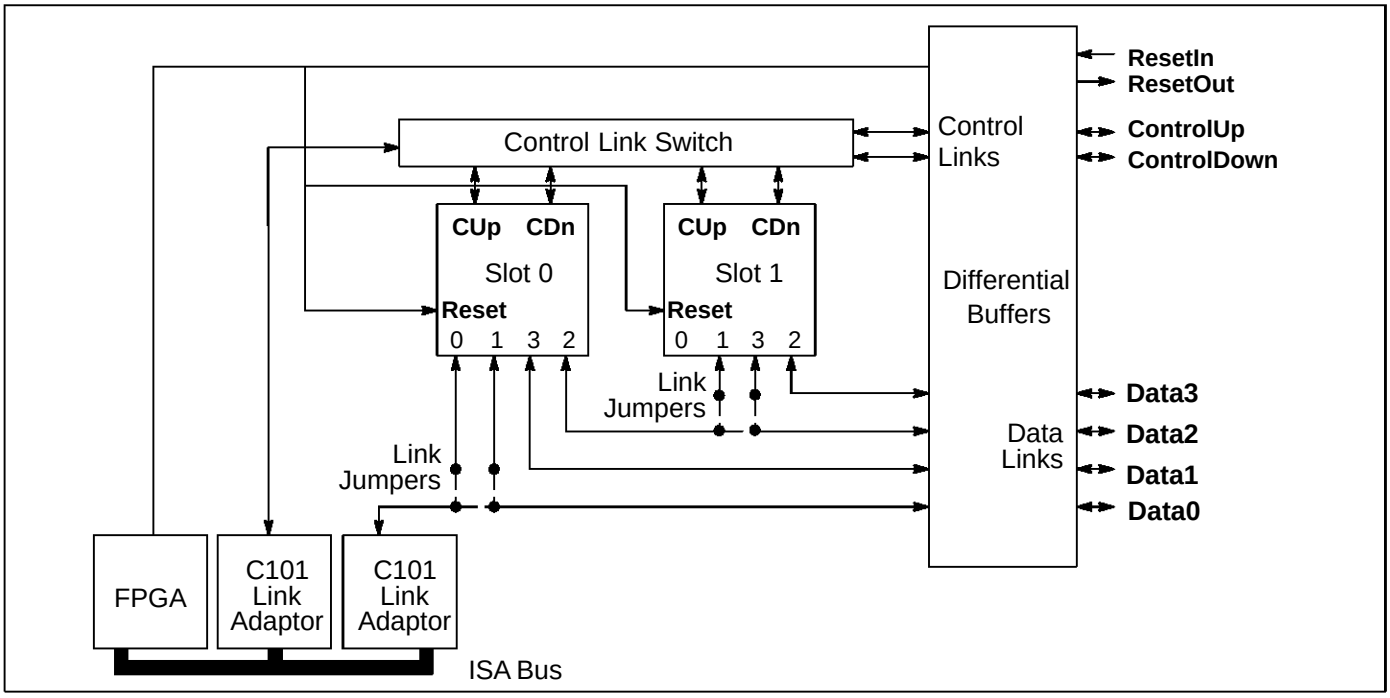

Figure 1.1 Block diagram of the IMS B108 hardware

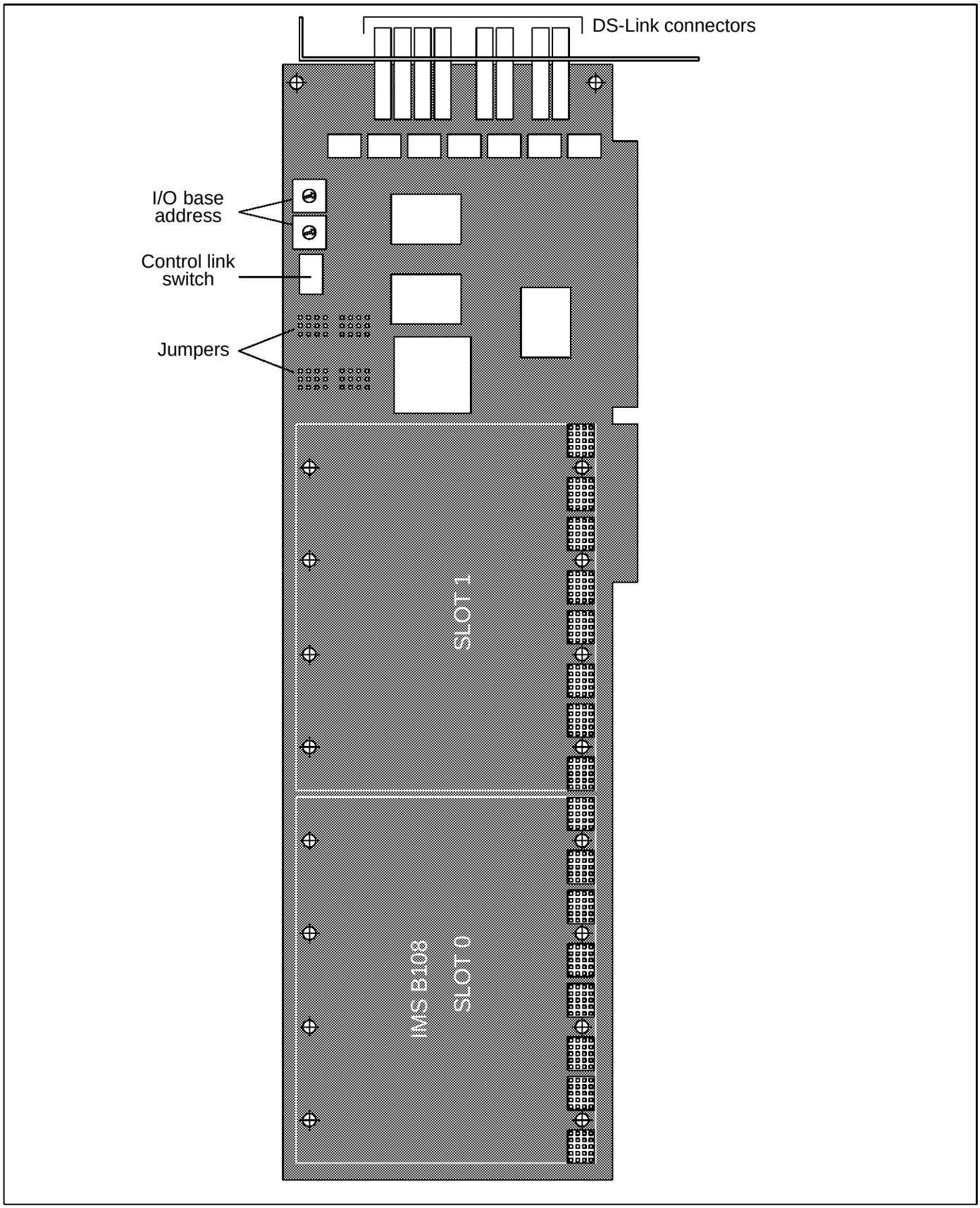

Figure 1.2 IMS B108 – board layout

1.1.1 PC bus and DS-Link interfaces

The bus interface on IMS B108 provides the following functions:

- Interfaces two ST C101 link adaptors to the PC-AT bus to provide the control and data DS-links.
- Provides support for hardware reset of the ST C101s, the HTRAM slots and/or an external network.
- Provides register selection of the PC interrupt line used by the ST C101 interface.

These functions are accessed via registers mapped into the I/O address space of the PC-AT bus. The memory map for the bus interface is shown in table 1.1. The addresses shown in the table are the byte I/O addresses of the various registers above a user-definable base address. This base address can be set by SW2 and SW3 on the board to any 32 byte boundary between the I/O addresses #020 and #3FF. These switches can also be set to disable the bus interface altogether by selecting a base address of #000. Since the usable I/O address space is limited on the PC-AT the ST C101 register addresses have been re-mapped and not all of the ST C101 registers are directly accessible at any given time. In addition, only the registers of one of the two ST C101 devices are directly accessible at any given time. The ST C101s are operated in 16 bit bus mode with only those registers that have 16 significant bits will be mapped into the PC I/O address space as a 16 bit register. Of the remaining registers, only the least significant byte can be read. A zero value will be written into the most significant byte of these registers on a write operation.

The specific ST C101 device to be accessed at any given time is switched by a bit in the **BoardControlRegister**, (refer to table 1.2). This selection bit switches all of the registers in table 1.1 that are *not* marked with an *. With the arrangement as designed, it is possible to monitor the interrupt status of the control link ST C101 on a continuous basis whilst the majority of the user I/O accesses are to the data link ST C101 registers. This reflects the anticipated normal mode of interface operation after booting a T9000 network.

Note that to ensure correct operation of the bus interface and the ST C101 devices, programmers must ensure that any I/O accesses to registers marked as 16 bit in table 1.1 are 16 bit accesses. Accesses to registers marked as 8 bit in table 1.1 should only be 8 bit accesses.

Name	Address	Register size/bits
LinkData8	0	8
LinkData16	2	16
TxSendPacket	4	16
TxPacketHeaderLower0	6	16
TxPacketHeaderUpper0	8	16
TxPacketHeaderLower1	A	16
TxPacketHeaderUpper1	C	16
RxPacketHeaderLower	E	16
RxPacketHeaderUpper	10	16
RxPacketLength	12	8
TxHeaderLength0	13	8
TxHeaderLength1	14	8
TxInterruptStatus	15	8
RxInterruptStatus	16	8
TxInterruptEnable	17	8
RxInterruptEnable	18	8
RxAcknowledge	19	8
ControlTxInterruptStatus *	1A	8
ControlRxInterruptStatus *	1B	8
BoardControlRegister *	1C	8
IndexRegister *	1D	8
DataRegister *	1E	16

Table 1.1 IMS B108 PC I/O address space memory map

Base address switches SW2 and SW3

The I/O addresses used by the IMS B108 register bank are selected by SW2 and SW3. Values from #020 to #3E0 (Hex) can be used as the base address of this bank. Selecting #000 will disable the interface to the ISA bus. In an ISA bus PC only values from #100 to #3E0 and #000 should be selected to avoid clashes with the system board I/O devices. SW2 selects the most significant hex digit of the base address and SW3 the middle hex digit. If SW2 is set to X and SW3 is set to Y then the base address for the register bank is #XY0. Note the hex digit selected by SW2 must be even (0, 2, ... E) or incorrect operation of the bus interface will result.

ST C101 registers

Details of the operation of the ST C101 can be found in [5].

Board control register

This register contains seven bits which are used to control and configure the board hardware and read the **ResetAck** signal from an external network. Table 1.2 shows the allocation bits in the register and describes the function of each. All bits of the register are read/write with the exception of the **ResetAck** bit, bit 1, which is read only.

Interrupts

Selection of the ISA bus interrupt line to be used is performed via the **IRQ** selection bits in the **BoardControlRegister**, (table 1.2). **IRQ3**, **5**, **11**, or **15** can be selected by setting one of the specified bits. No **IRQ** line is driven if none of the selection bits are set high in this register. The state of the selected **IRQ** line on the ISA bus will be the result of an OR of the two **Int** signals from the ST C101 devices, if either device requests an interrupt the **IRQ** line will be set high. Refer to ISA bus documentation and the ST C101 data sheet, [5], for more information on the generation and handling of interrupts.

Bit number	Function	Description
0	**Reset**	Setting this bit to a 1 resets the ST C101 devices, the HTRAMs in the slots, and an external network connected to the **notResetOut** connector. The timing of setting and resetting this bit should be as defined in [6].
1	**ResetAck**	This bit allows the **ResetAck** signal on the **notResetOut** external connector to be read. See [6].
2	**IRQ3Sel**	Setting this bit high selects the **IRQ3** line on the ISA bus to be used for interrupts from the ST C101s.
3	**IRQ5Sel**	Setting this bit high selects the IRQ5 line on the ISA bus to be used for interrupts from the ST C101s.
4	**IRQ11Sel**	Setting this bit high selects the **IRQ11** line on the ISA bus to be used for interrupts from the ST C101s.
5	**IRQ15Sel**	Setting this bit high selects the **IRQ15** line on the ISA bus to be used for interrupts from the ST C101s.
6	**DevicePage**	This bit selects which ST C101 devices registers are accessable in the mapped register area. Setting this bit to a 0 selects the data ST C101, setting it to a 1 selects the control ST C101.
7	Reserved	Must be written with a 0. Will read back 0.
Note: Only one IRQ selection bit should be high at a time.		

Table 1.2 Board control register

Index register

Even with the device selection mechanism, not all of the ST C101 registers are mapped into the PC bus address space. An index and a data register mechanism is provided to access the remaining registers. To access a specific ST C101 register, the address of the register as defined in the ST C101 data sheet, [5], is ORed with the **IndexRegister** device selection bit and written into the **IndexRegister**. Any subsequent read or write operations to the **DataRegister** will result in read or write accesses to the selcted ST C101 register. These accesses are always 16 bit transfers.

Bit number	Function	Description
4–0	**C101A0–4**	C101 address bits 4–0 for accesses through **Data** register
5	**DeviceSelection**	Selects device to be accessed through **Data** register 0 = C101 **Data** 1 = C101 **Control**
6	Reserved	
7	Reserved	

Table 1.3 Index register

1.1.2 HTRAM slots and data link network

There are two logical slots on the IMS B108, both of size 4. This allows up to two HTRAMs to be supported. The control links are arranged to allow support of HTRAMs of size 2 or 4 in each slot.

Care needs to be taken to ensure that the total power taken by the IMS B108 and the HTRAMs plugged onto the board do not exceed the total power available on an ISA slot of 22.5W. The power taken by the IMS B108 is 8W. Refer to individual HTRAM datasheets for their power consumptions.

The data links between HTRAM slots on the IMS B108 are connected as shown in figure 1.3

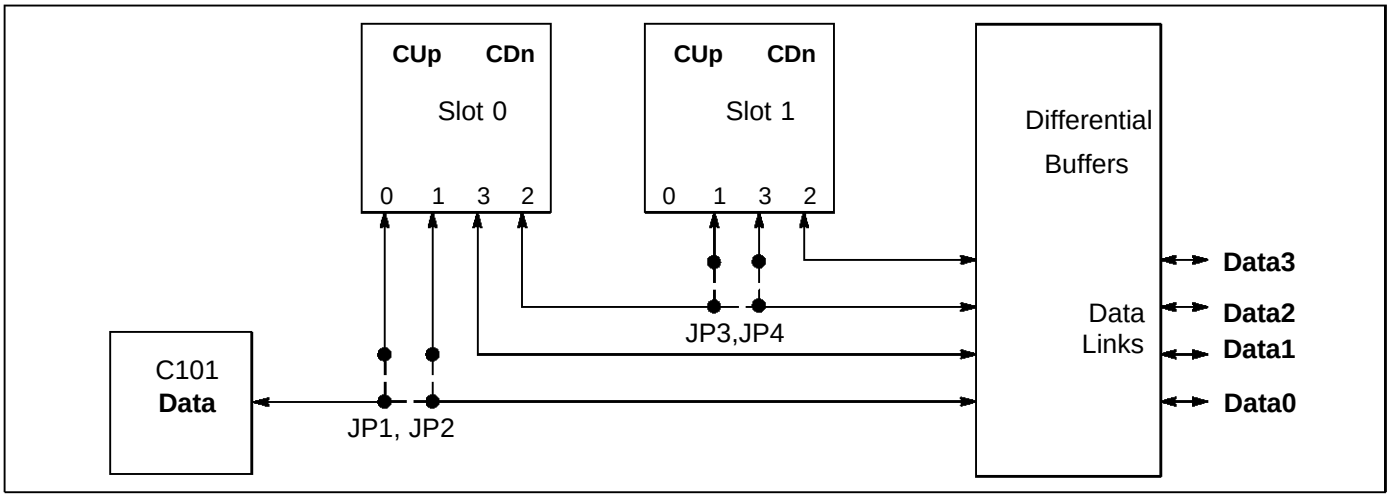

Figure 1.3 Data link connections between HTRAM slots

Data link jumpers, JP1–4

Jumpers JP1-4 enable reconfiguration of a small number of the data links from the two HTRAM slots and the data link ST C101. The jumpers must be used in pairs, JP1 with JP2, and JP3 with JP4. Each

pair of jumpers can be in two positions, all jumpers towards the inside of a line drawn between the centers of the pins, or all jumpers towards the outside of the pins — an example is shown in figure 1.4.

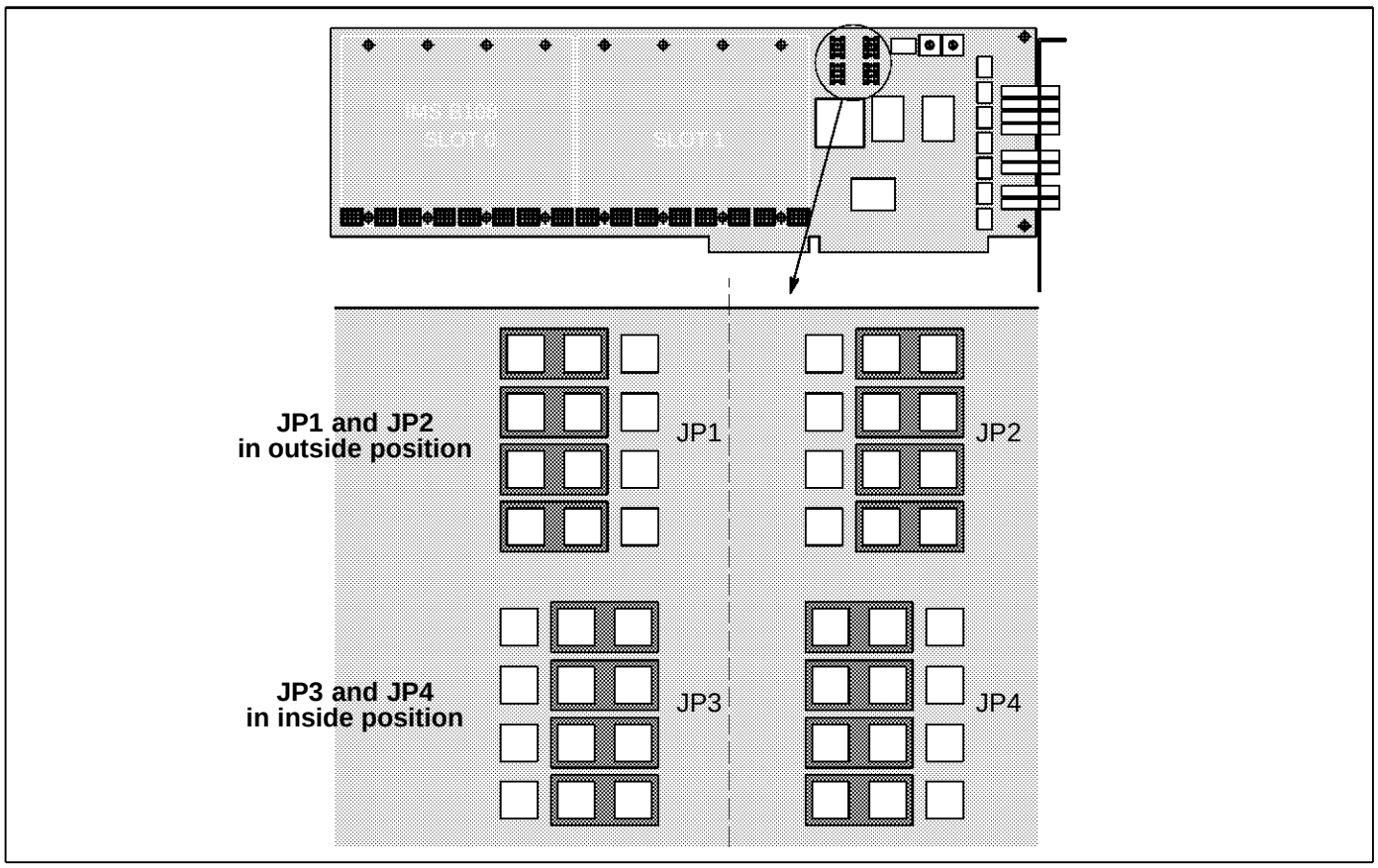

Figure 1.4 Jumper positions

Jumper positions and the selected connections are given in table 1.4.

Jumper	Positions	Connection(s)
JP1 and JP2	Inside	C101 **Data** to **Data0** SLOT 0 Links 0 and 1 N/C
JP1 and JP2	Outside	C101**Data** to SLOT 0 Link 0 SLOT 0 0 Link 1 to **Data0**
JP3 and JP4	Inside	SLOT 0 Link 2 to **Data2** SLOT 1 Links 1 and 3 N/C
JP3 and JP4	Outside	SLOT 0 Link 2 to SLOT 1 Link 1 SLOT 1 Link 3 to **Data2**

Table 1.4 IMS B108 JP1–4 connections

1.1.3 Control link network

The control links on the IMS B108 are connected into a pipeline with options on connection of the head of the pipeline and bypassing (jumping over) slots. Figure 1.5 shows the general arrangement

of the control links on the IMS B108. All control link connections are taken to a control link switch device, with the actual control link connections on the board selected by SW1. **ControlUp** and **ControlDown** links are taken to differentially buffered connectors on the back panel.

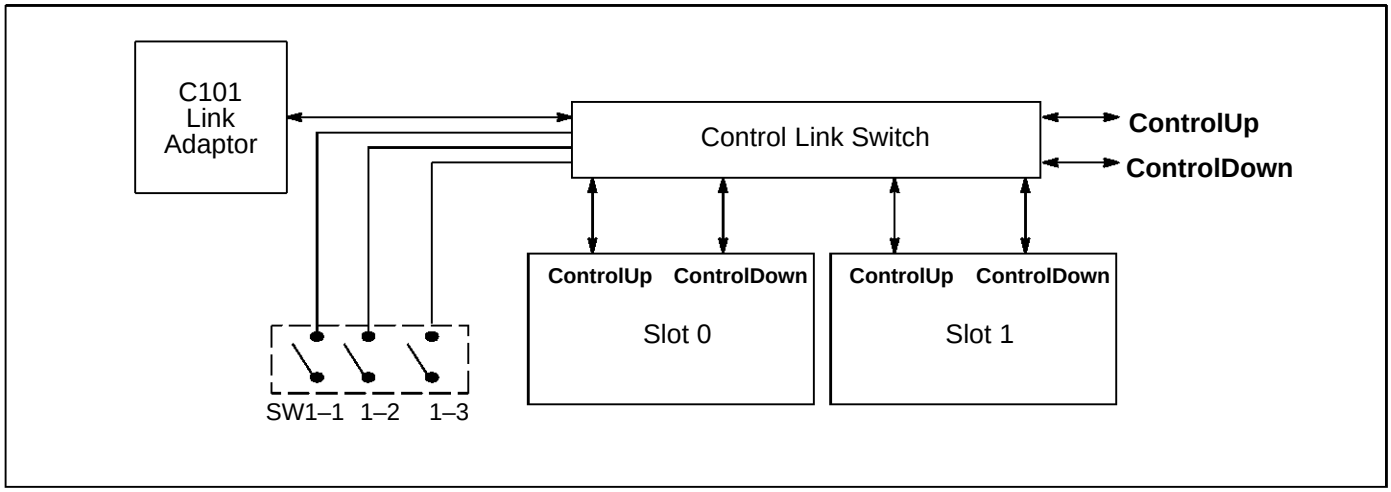

Figure 1.5 Control links on IMS B108

Control link switch, SW1

The functions of the switches are marked around SW1 in mnemonic form. SW1–1 is marked with an **H** for Host (C101 **Control**), and **U** for **ControlUp** connected to the head of the pipeline. SW1–2 is marked **J0** for jump over Slot 0. SW1–3 is marked **J1** for jump over Slot 1. The bar of the dip-switch should be slid towards the side of the switch where the mnemonic is located, in order to make the associated connections.

The connections made by the combinations of these three switches are shown in table 1.5.

Note:
Due to the switching arrangement of the control links on the IMS B108, it is not possible to run the T9000 control network reliably at speeds of greater than 50Mbit/s. This restriction should be reflected in the Network Description Language files for the system.

SW1-1	SW1-2	SW1-3	Connection(s)
ON	ON	ON	External **ControlUp** to SLOT 0 **ControlUp** SLOT 0 **ControlDown** to SLOT 1 **ControlUp** SLOT 1 **ControlDown** to external **ControlDown**
ON	ON	OFF	External **ControlUp** to SLOT 0 **ControlUp** SLOT 0 **ControlDown** to external **ControlDown** SLOT 1 **ControlUp** and **Down** N/C (SLOT 1 jumped)
ON	OFF	ON	External **ControlUp** to SLOT 1 **ControlUp** SLOT 1 **ControlDown** to external **ControlDown** SLOT 0 **ControlUp** and **Down** N/C (SLOT 0 jumped)
ON	OFF	OFF	External **ControlUp** to external **ControlDown** SLOT 0 **ControlUp** and **Down** N/C (SLOT 0 jumped) SLOT 1 N/C **ControlUp** and **Down** (SLOT 1 jumped)
OFF	ON	ON	C101 **Control** to SLOT 0 **ControlUp** SLOT 0 **ControlDown** to SLOT 1 **ControlUp** SLOT 1 **ControlDown** to external **ControlDown**
OFF	ON	OFF	C101 **Control** to SLOT 0 **ControlUp** SLOT 0 **ControlDown** to **ControlDown** external SLOT 1 **ControlUp** and **Down** N/C (SLOT 1 jumped)
OFF	OFF	ON	C101 **Control** to SLOT 1 **ControlUp** SLOT 1 **ControlDown** to external **ControlDown** SLOT 0 **ControlUp** and **Down** N/C (SLOT 0 jumped)
OFF	OFF	OFF	C101 **Control** to external **ControlDown** SLOT 0 **ControlUp** and **Down** N/C (SLOT 0 jumped) SLOT 1 **ControlUp** and **Down** N/C (SLOT 1 jumped)
Note: SW1-4 is not used.			

Table 1.5 IMS B108 control link switch connections

1.1.4 External connections

Four data links, **Data0–3**, the **ControlUp**/**Down** links, and the external **notReset** signals are all buffered using AT&T 41 series differential buffers and brought out to the backpanel on DS-Link modular connectors. The assignment of these backpanel connectors is shown in figure 1.6. These connections conform to the standards for DS-Links and external resets which can be found in [6].

These external connections allow several IMS B108s with HTRAMs to be connected into a network using one IMS B108 as the host interface. To achieve this interconnection external DS-Link cables should be used to daisy chain the **ControlUp/Down** and the **notResetIn**/**Out** connections in between boards, as shown in figure 1.7.

An IMS B108 can also be used as an interface between a PC and an external T9000 network, as in figure 1.8, by connecting cables to the **ControlDown** and one of the data links, **Data0–3**. In the case where no HTRAMs are used on the IMS B108 itself, (i.e. it is being used purely as an interface card), the data link connection will be to **Data0** and the data link jumpers will need to be appropriately set, (JP1 and JP2 on the ‘inside’ position), and the control link switches SW1-1 to SW1–3 should be in the ‘off’, position. Refer to table 1.5.

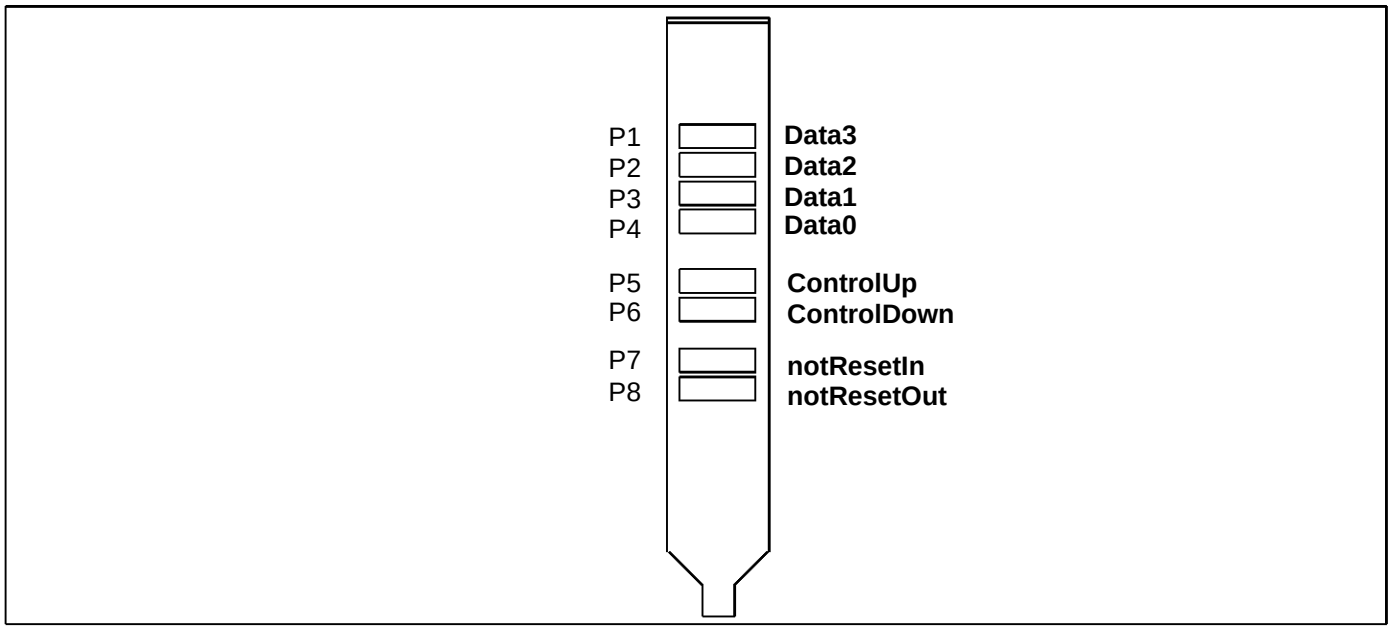

Figure 1.6 IMS B108 rear panel connections

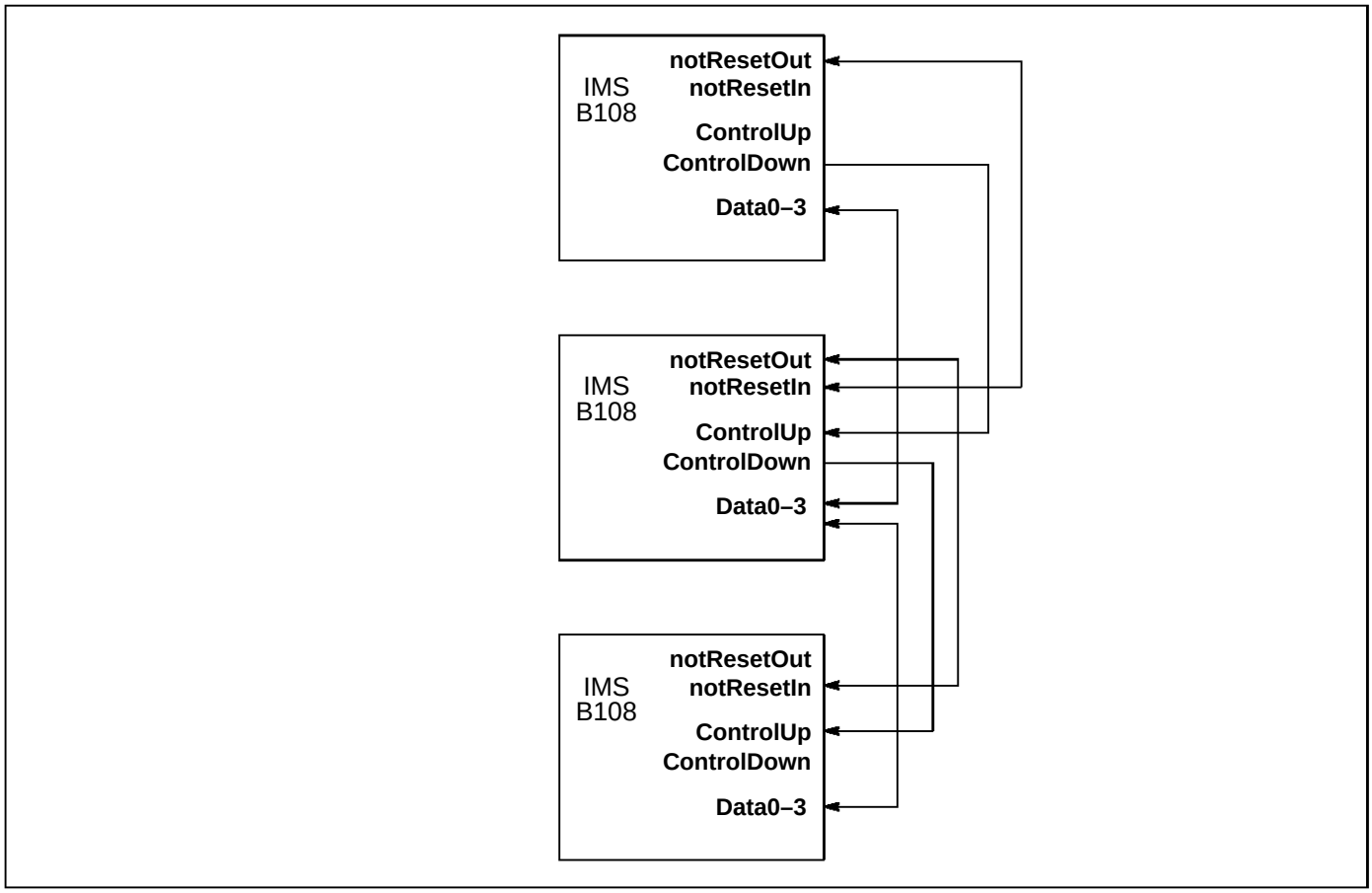

Figure 1.7 IMS B108 interconnection daisy chain

Board reset signals

Use of the **notResetOut** signal allows the PC to reset the external hardware under software control.

A **notResetIn** signal to the board is inverted, ORed with the reset generated from the **BoardControlRegister**, and resets both the ST C101s and the HTRAM slots. It is then propagated to the **notResetOut** connector. The **notResetAck** signal on the **notResetIn** connector is driven active low when the **notReset** signal on the **notResetIn** connector is active low.

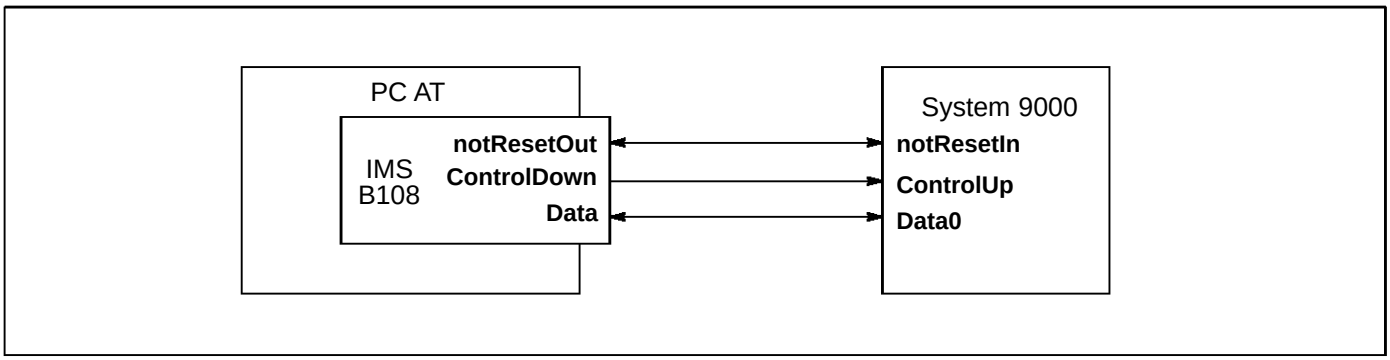

Figure 1.8 IMS B108 interface between a PC and an external T9000 network

1.2 Software support

Software support for the IMS B108 is provided by the IMS S7398.

1.3 Product documentation

1.3.1 Installation and user manual

A user manual is provided, which describes how to install, set up, and use the IMS B108 and its associated interface software. This also outlines how to build and run example applications on the IMS B108 and HTRAM networks.

1.4 Electrical and thermal requirements

1.4.1 Cooling requirements

Adequate air cooling must be provided to ensure that any HTRAMS fitted to the motherboard are kept within their operating temperature range. Failure to do so may affect the reliability of the HTRAMS. Air flow should run parallel to the board surface and parallel to the length of the IMS B108.

The cooling airflow requirements for the IMS B108 itself are defined in table 1.6. The datasheets for individual HTRAMs should be consulted to determine the system cooling requirements.

It should be noted that PC airflow ranges are typically 0 – 0.5m/s.

1.4.2 Operating Ranges

Functionality is not guaranteed outside the Operating Ranges. Operation beyond the Operating Ranges is not recommended and may affect device reliability.

Parameter	Min.	Typ.	Max.	Unit	Notes
Operating temperature	0		50	°C	
Airflow	0			m/s	1
+5V DC	4.75		5.25	V	
Power consumption (+5V DC)			8	W	2

1 It should be noted that adequate cooling airflow must be provided to maintain any fitted HTRAMs within their rated operating temperature.

2 Value shown is with **no** HTRAMs fitted. Total power consumption of the motherboard plus HTRAMs must not exceed 22.5W.

Table 1.6 Operating Ranges

1.4.3 Absolute maximum ratings

Functionality at or above these limits is not implied. Stresses beyond the absolute maximum ratings may cause permanent damage.

Parameter	Min.	Max.	Unit
Storage temperature	0	70	°C
Supply Voltage	0	7.0	V

Table 1.7 Absolute maximum ratings

1.5 Ordering information

Description	Order number
IMS B108 PC HTRAM motherboard	IMS B108-1

1.6 Field support

INMOS products are supported worldwide through SGS-THOMSON Sales Offices and authorised distributors.

1.7 References

1 *T9000 Transputer Hardware Reference Manual,* INMOS Ltd 1993

2 *HTRAM specification*, INMOS Ltd 1994

3 *T9000 Brochure,* INMOS Ltd 1993

4 *IMS Dx394 T9000 ANSI C Toolset datasheet,* INMOS Ltd, 1994
IMS Dx395 T9000 occam 2 Toolset datasheet, INMOS Ltd, 1994
IMS Dx390 T9000 INQUEST datasheet, INMOS Ltd, 1993

5 *ST C101 DS-Link Adaptor Datasheet*, INMOS Ltd 1994

6 *DS–Link Connector Standards and Cabling*, INMOS Ltd 1994, (42 1634 00)